


Regarding the usage of our schematics and alike documentation for Trenz module AM0010.

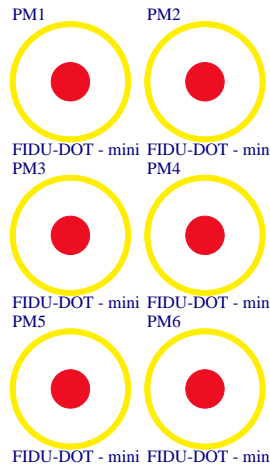
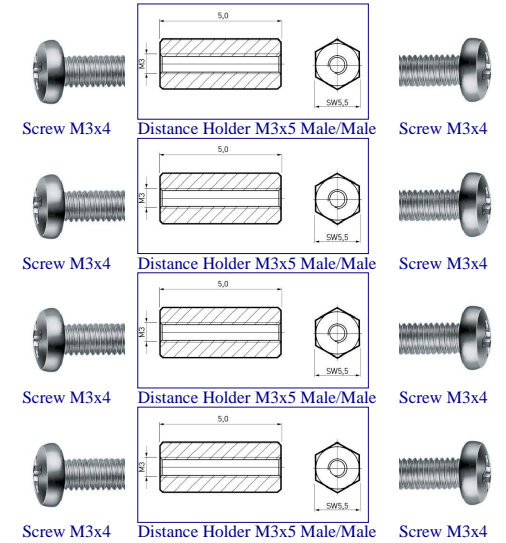
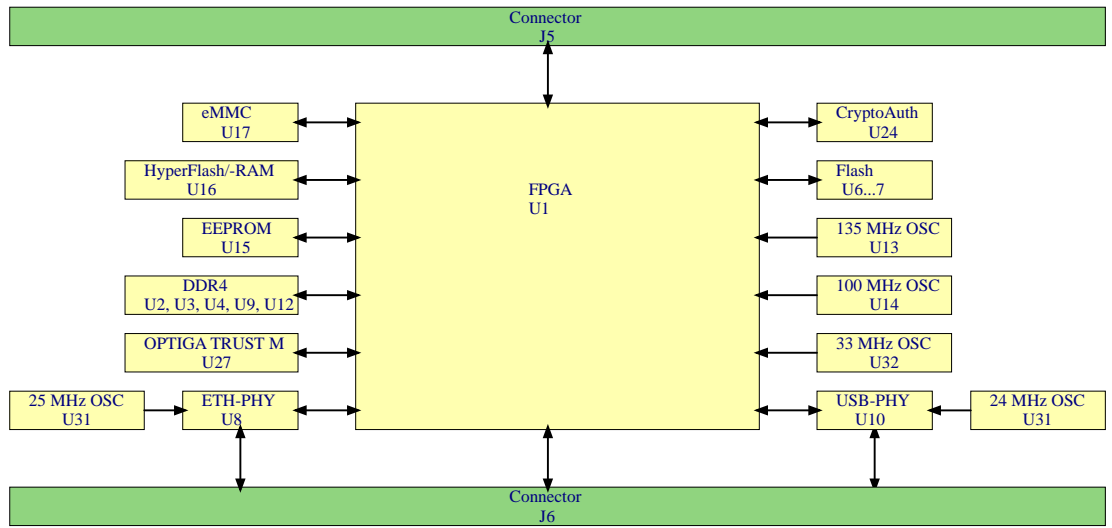
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. AM0010 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

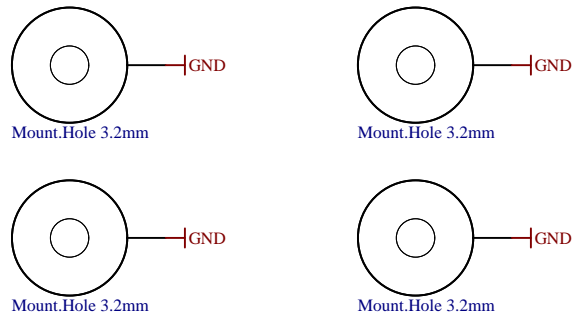
	Title: AM0010 – Legal Notices Modules		
	A4	Number: Legal Notices Modules [No Variations]	Rev. 01
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 1 of 30
	Filename: Legal Notices Modules.SchDoc		

Special notes:

- | | |
|---|---|
| U_B2B_Connector_1
B2B_Connector_1.SchDoc | U_POWER_1
POWER_1.SchDoc |
| U_B2B_Connector_2
B2B_Connector_2.SchDoc | U_POWER_2
POWER_2.SchDoc |
| U_MPSoC
MPSoC.SchDoc | U_REV_CH
Revision_Changes.SchDoc |
| U_DDR4-RAM
DDR4-RAM.SchDoc | U_Legal_Notices_Modules
Legal_Notices_Modules.SchDoc |
| U_DDR4-RAM_2
DDR4-RAM_2.SchDoc | |
| U_DDR4-RAM_3
DDR4-RAM_3.SchDoc | |
| U_DDR4-RAM_4
DDR4-RAM_4.SchDoc | |
| U_DDR4-RAM_5
DDR4-RAM_5.SchDoc | |
| U_DDR4-CAPS
DDR4-CAPS.SchDoc | |
| U_DDR4-TERM
DDR4-TERM.SchDoc | |
| U_ETHPHY
ETHPHY.SchDoc | |
| U_USBPHY
USBPHY.SchDoc | |
| U_eMMC
eMMC.SchDoc | |
| U_MISC
MISC.SchDoc | |



Serial
Serialnumber 6,3 x 6.3mm



Title: AM0010		
A4	Number: AM0010 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 2 of 30
Filename: AM0010.SchDoc		
Assembly variant [No Variations]		
Created by		
Modified by		
Modified at		
SVN Revision 457		

1

2

3

4

A

A

B

B

C

C

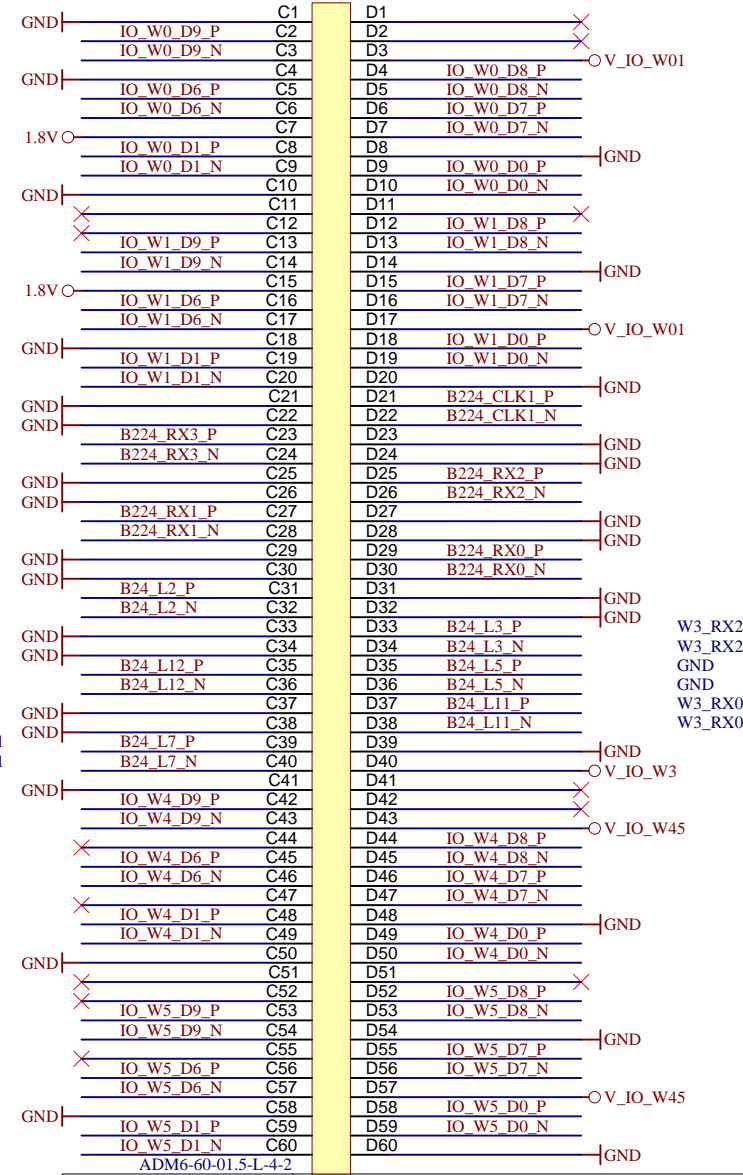
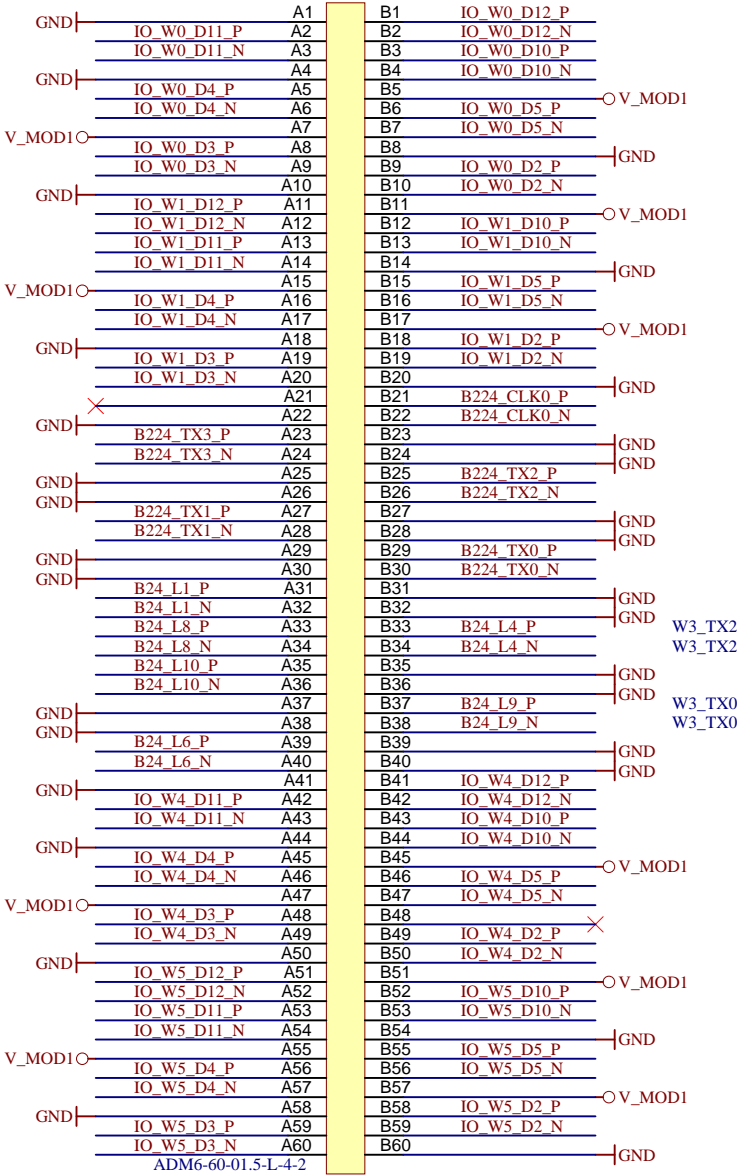
D

D

Connector W

J5A

J5B



W3_TX3
W3_TX3
GND
W3_TX1
W3_TX1

W3_CLK0
W3_CLK0

W3_TX2
W3_TX2

W3_TX0
W3_TX0

W3_RX3
W3_RX3

W3_RX1
W3_RX1

W3_CLK1
W3_CLK1

W3_RX2
W3_RX2
GND
W3_RX0
W3_RX0

W3_RX0
W3_RX0



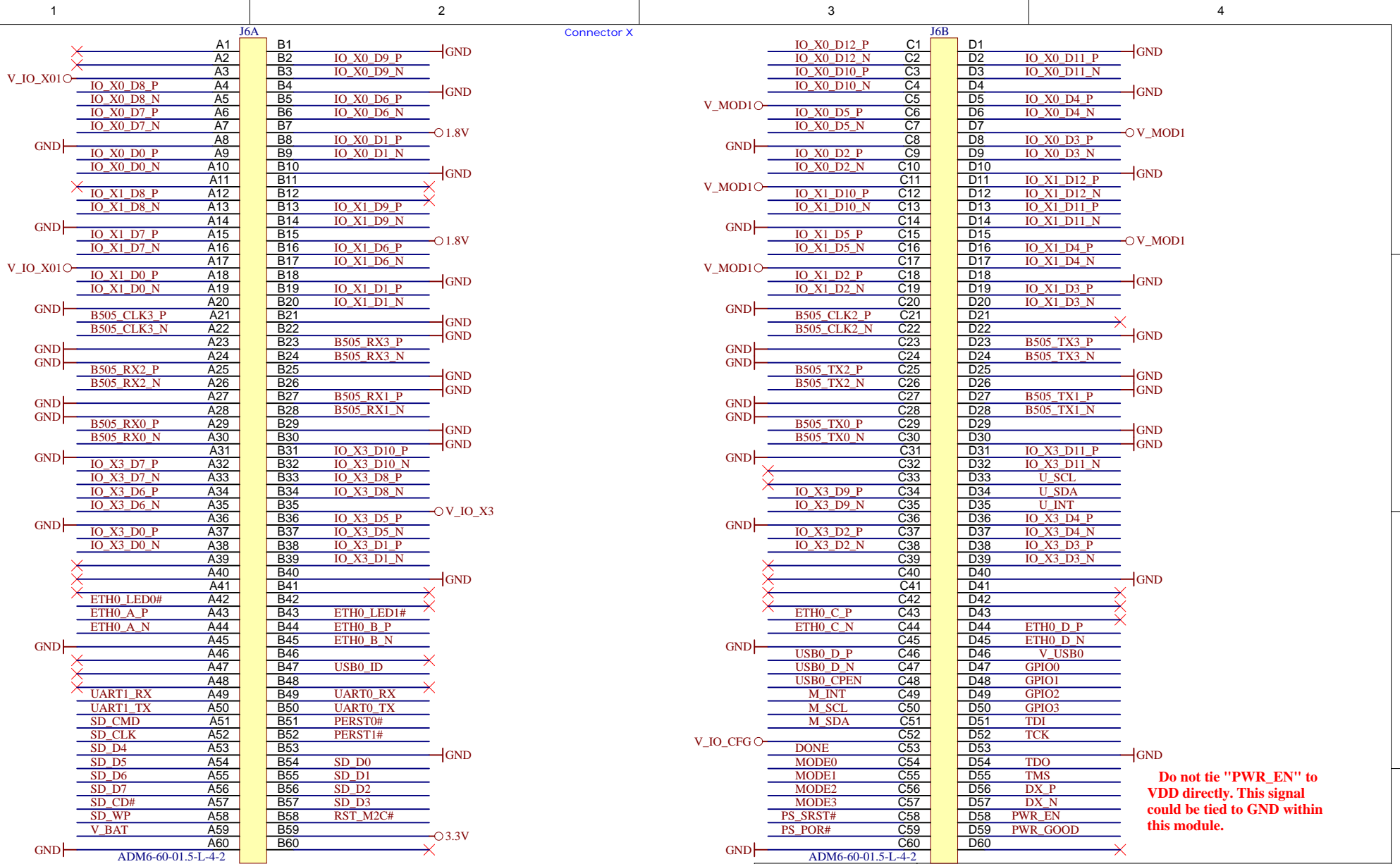
Title: AM0010 – B2B_Connector_1		
A4	Number: B2B_Connector_1 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 3 of 30
Filename: B2B_Connector_1.SchDoc		

1

2

3

4



Do not tie "PWR_EN" to VDD directly. This signal could be tied to GND within this module.



Title: AM0010 – B2B_Connector_2		
A4	Number: B2B_Connector_2 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 4 of 30
Filename: B2B_Connector_2.SchDoc		

1

2

3

4

A

A

B

B


C

C

D

D

- U_B64
B64.SchDoc
- U_B65
B65.SchDoc
- U_B66
B66.SchDoc
- U_B_HD
B_HD.SchDoc
- U_B_MIO
B_MIO.SchDoc
- U_PS_DDR
PS_DDR.SchDoc
- U_B_PS_GT
B_PS_GT.SchDoc
- U_B_GT
B_GT.SchDoc
- U_CONFIG
CONFIG.SchDoc
- U_ZU_POWER
ZU_POWER.SchDoc
- U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

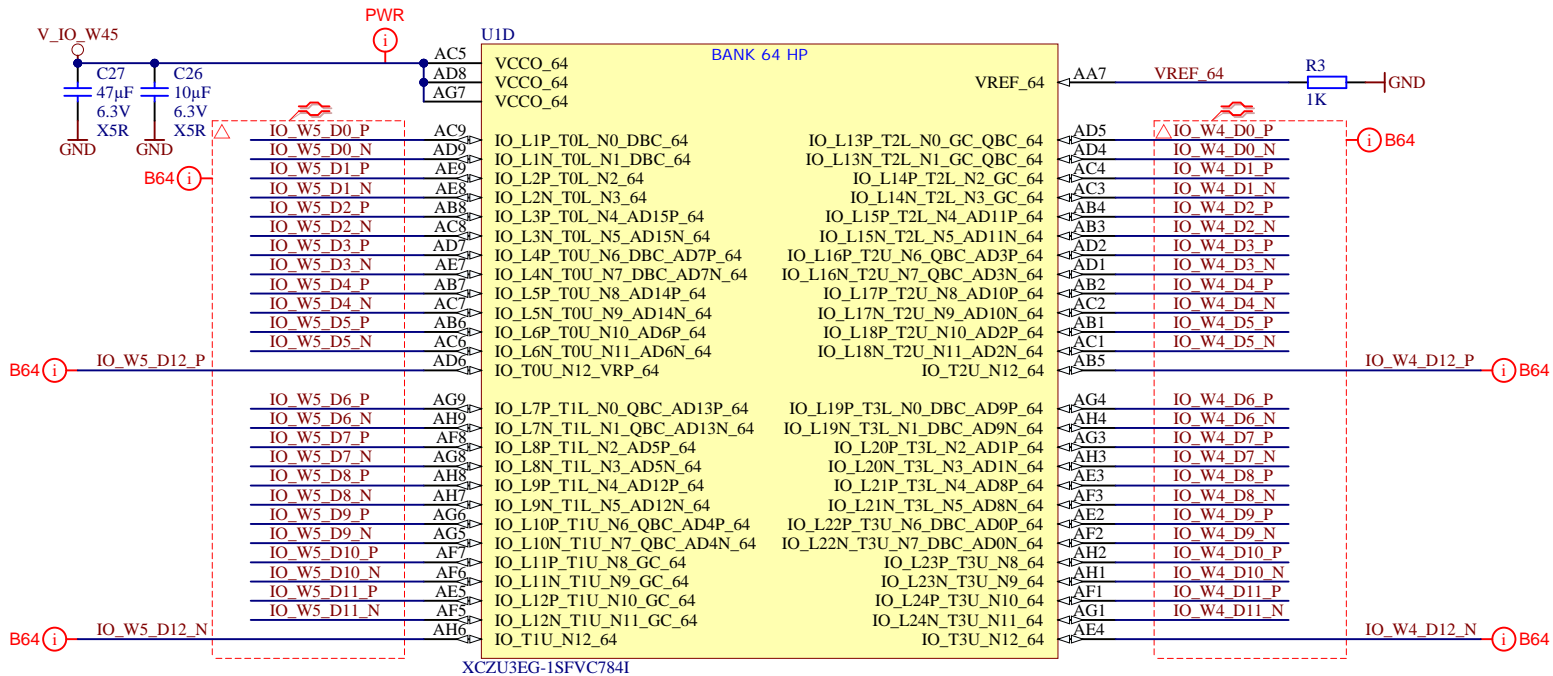
	Title: AM0010 – MPSoC		
	A4	Number: MPSoC [No Variations]	Rev. 01
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 5 of 30
	Filename: MPSoC.SchDoc		

1

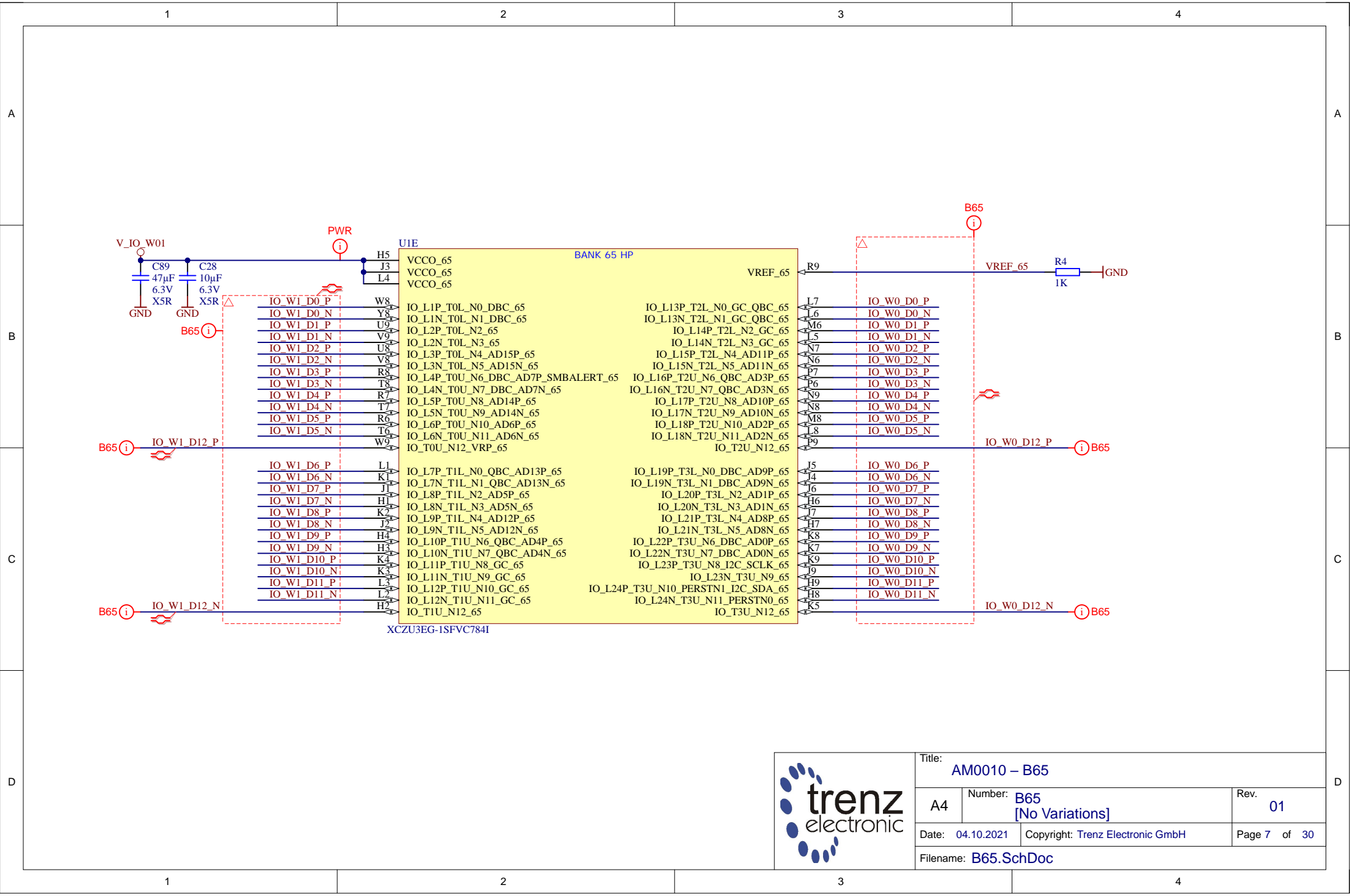
2


3

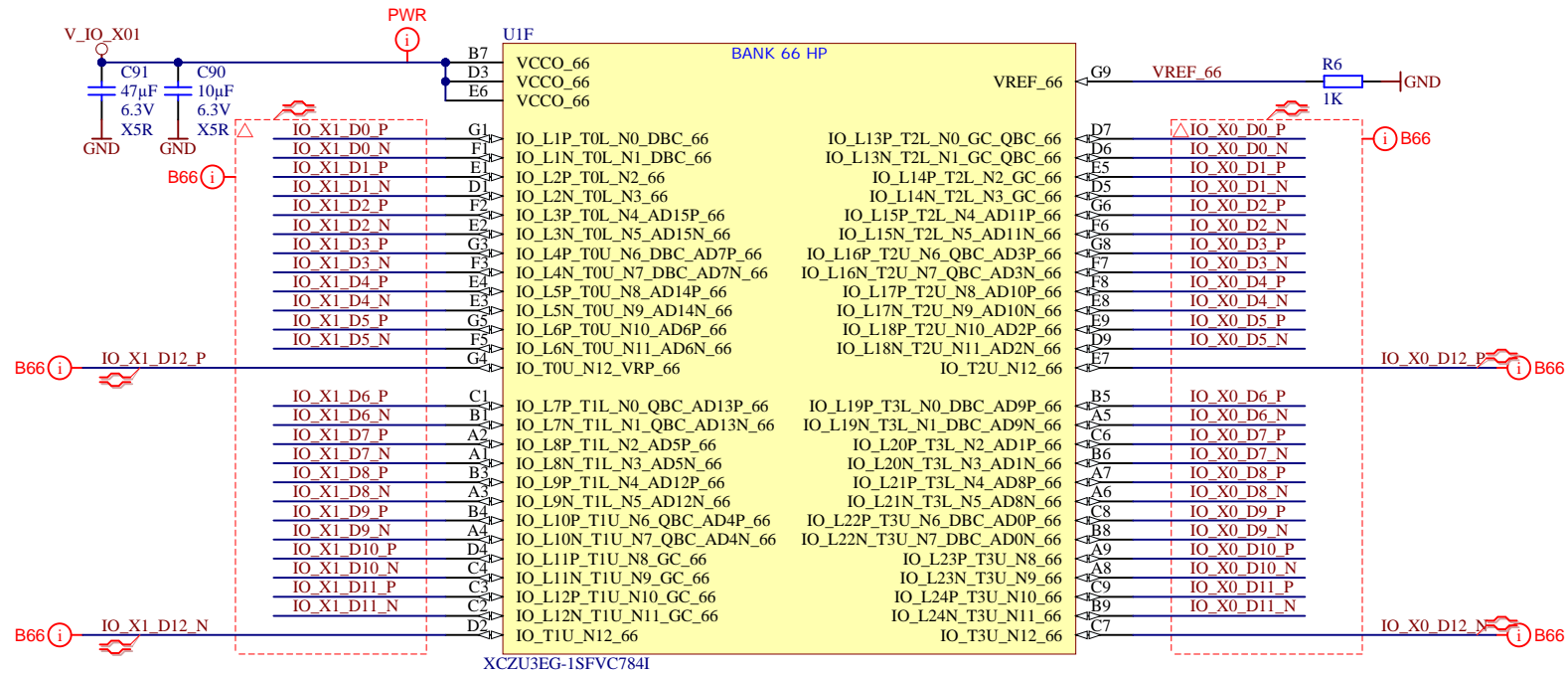
4



Title: AM0010 – B64		
A4	Number: B64 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 6 of 30
Filename: B64.SchDoc		



		Title: AM0010 – B65	
		A4	Number: B65 [No Variations]
Date: 04.10.2021		Copyright: Trenz Electronic GmbH	
Filename: B65.SchDoc		Rev. 01	
Page 7		of 30	



Title: AM0010 – B66		
A4	Number: B66 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 8 of 30
Filename: B66.SchDoc		

A

A

B

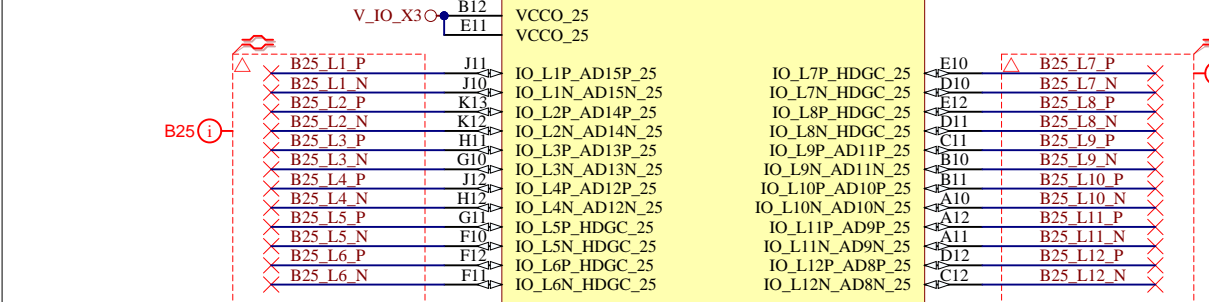
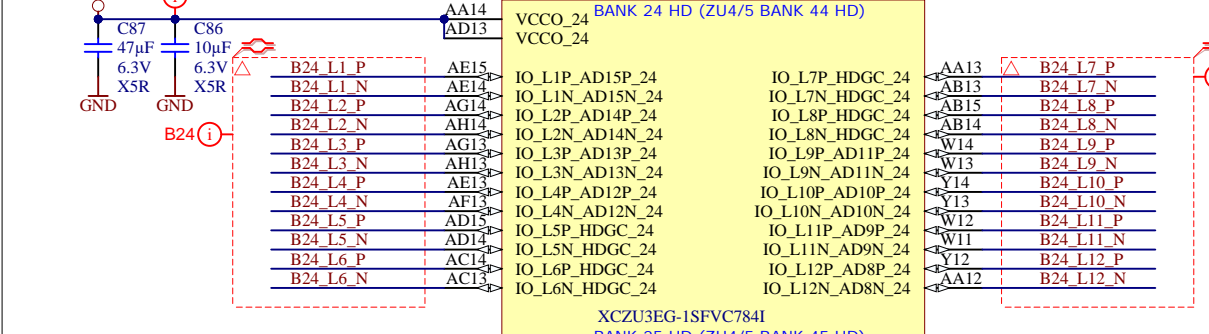
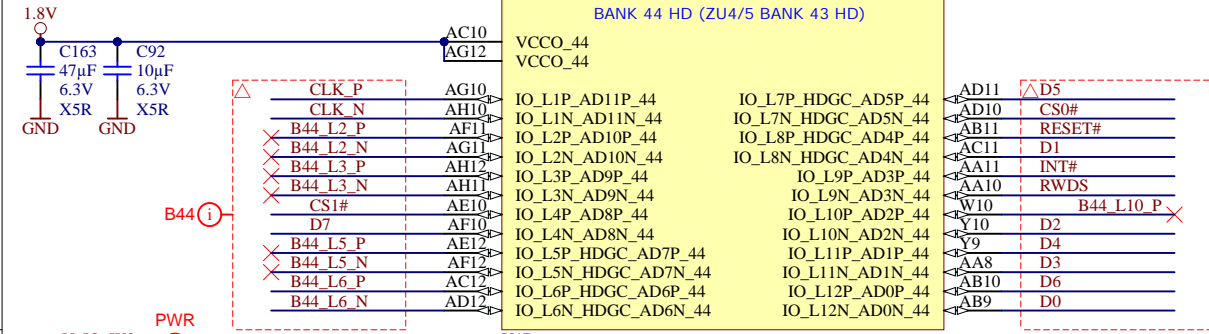
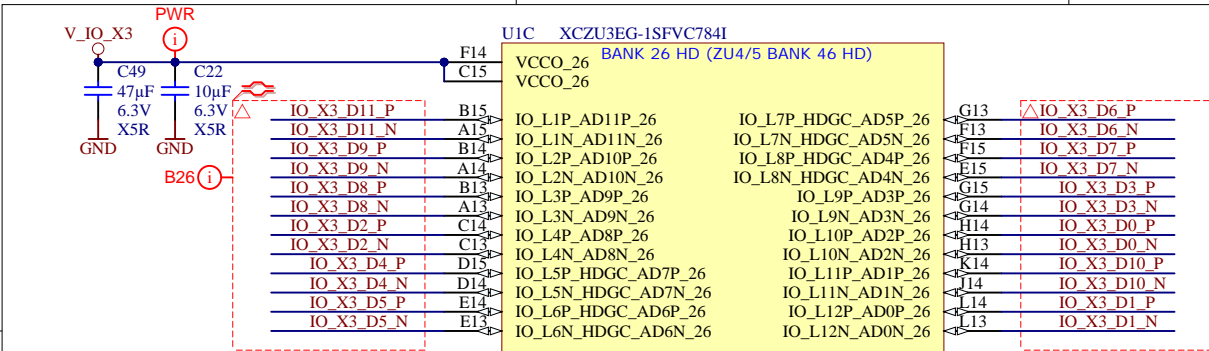
B

C

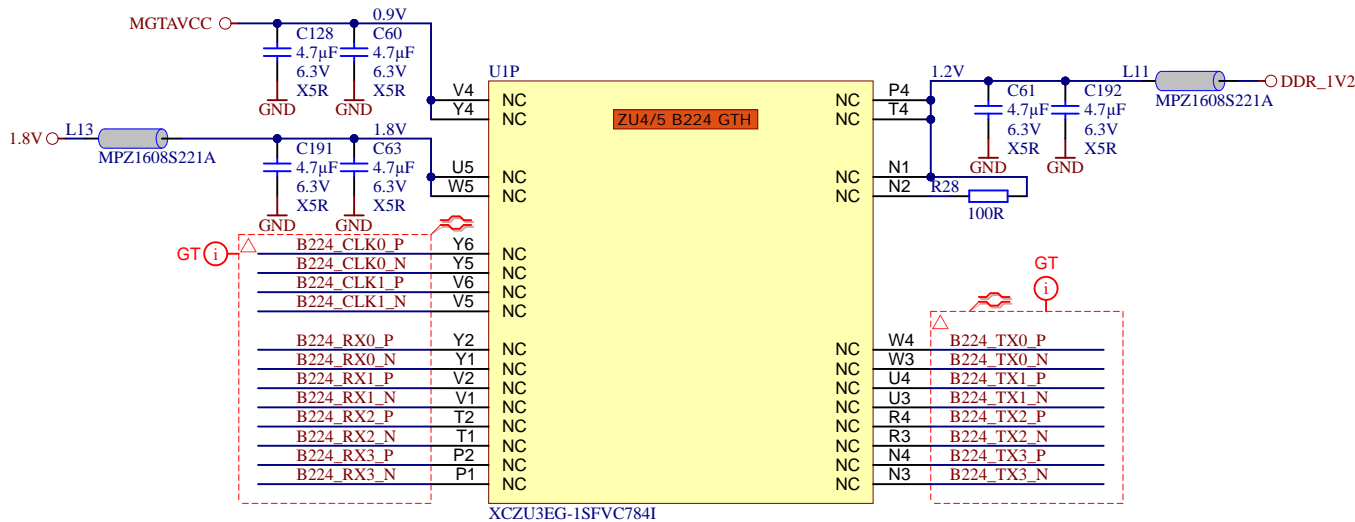
C

D

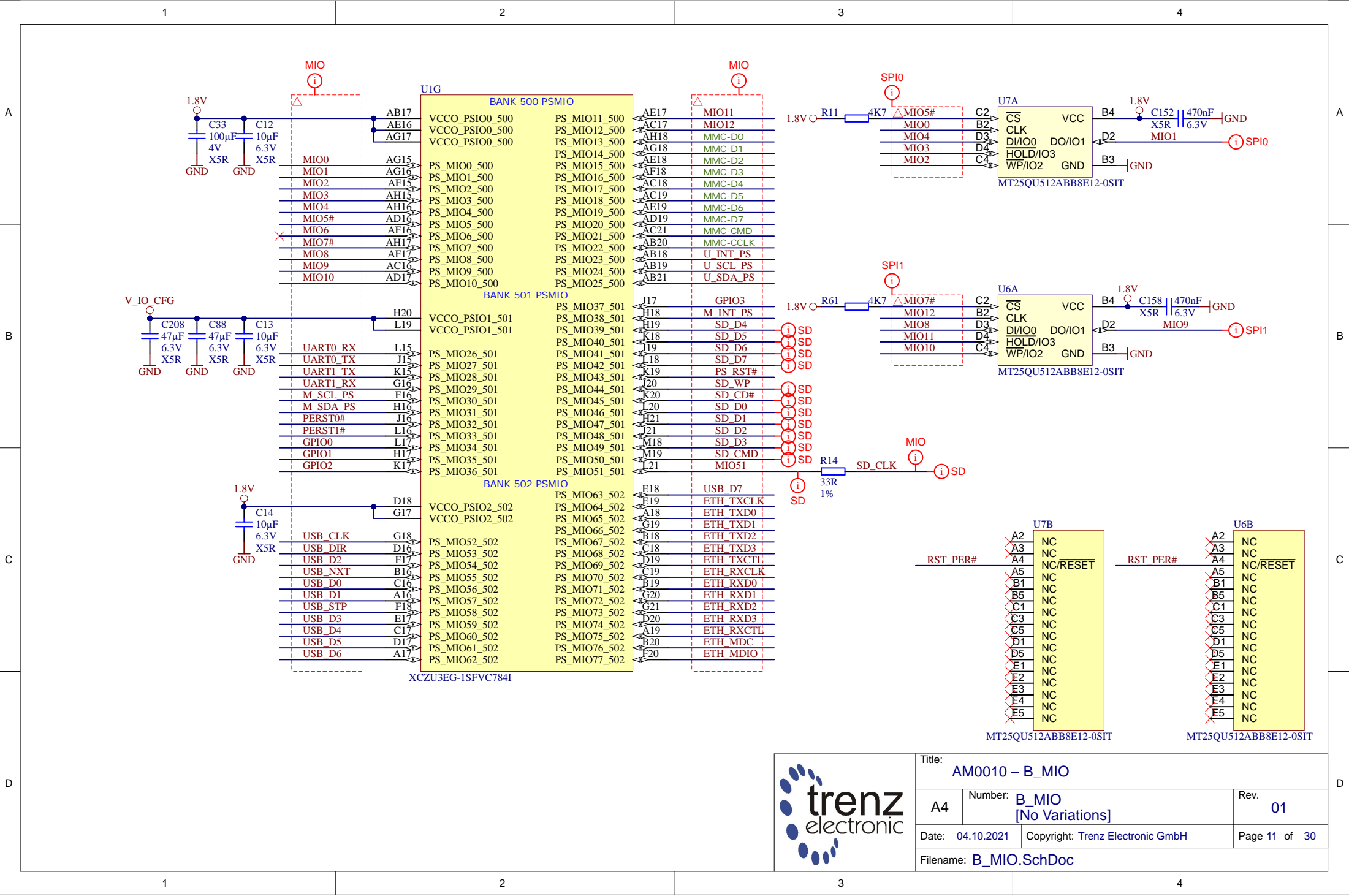
D



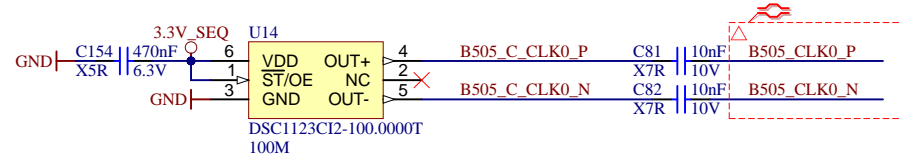
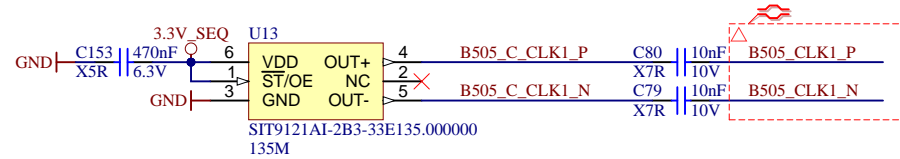
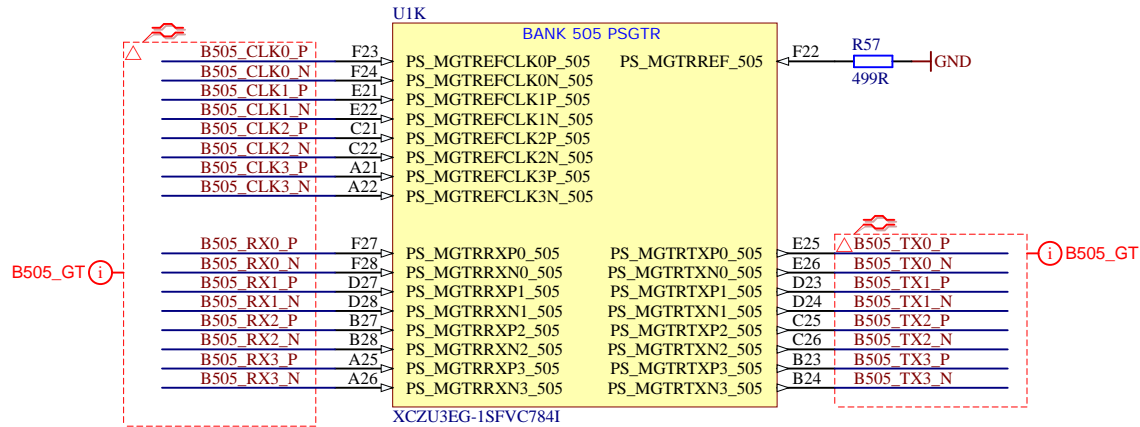
Title: AM0010 - B_HD		
A4	Number: B_HD [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 9 of 30
Filename: B_HD.SchDoc		



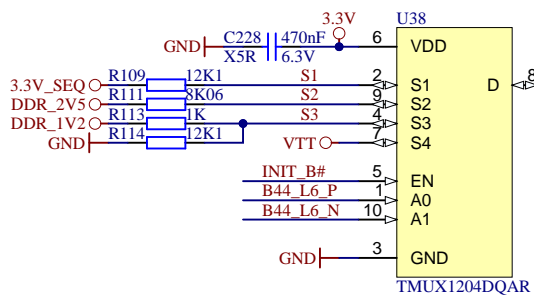
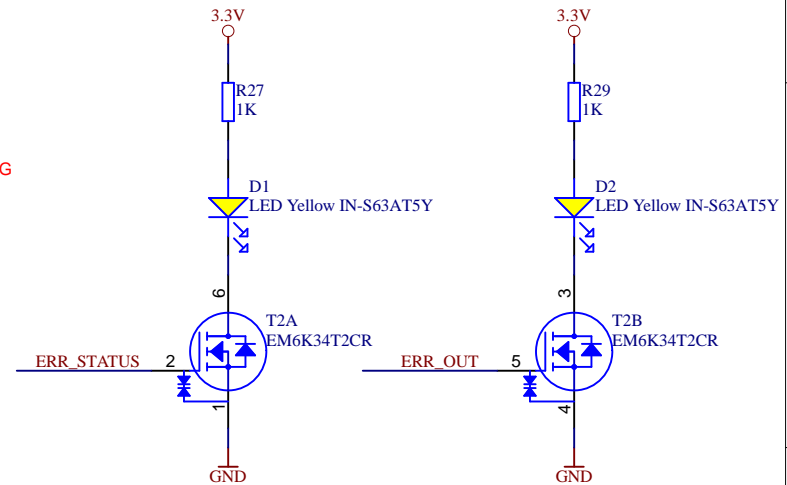
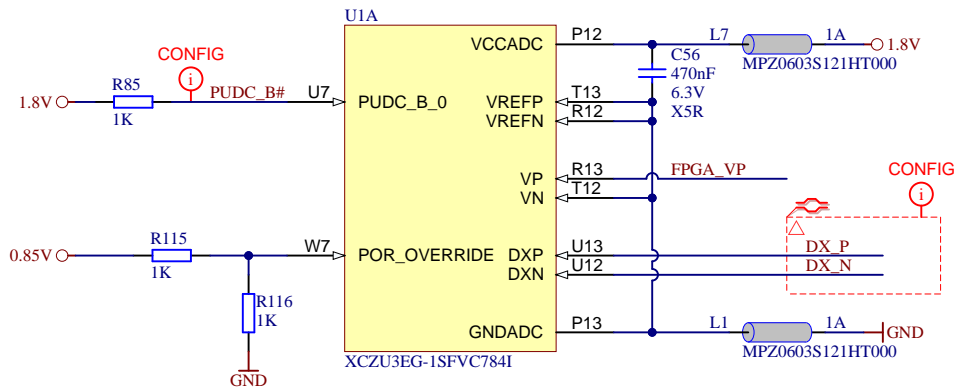
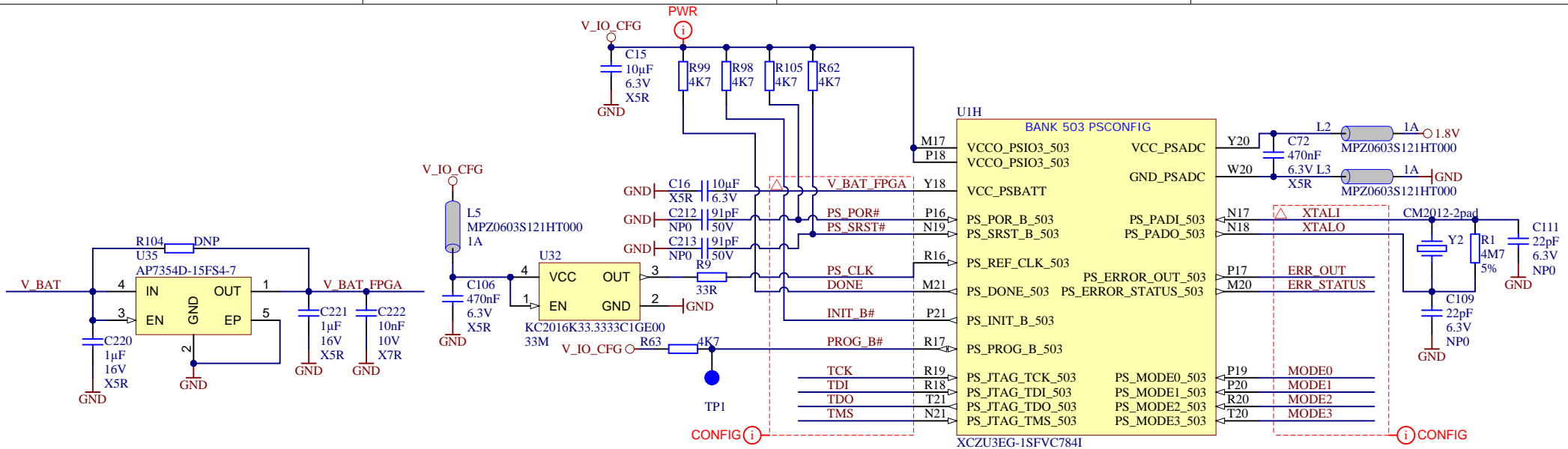
	Title: AM0010 - B_GT	
	A4	Number: B_GT [No Variations]
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH
	Filename: B_GT.SchDoc	
	Rev. 01	Page 10 of 30



	Title: AM0010 - B_MIO	
	A4	Number: B_MIO [No Variations]
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH
	Filename: B_MIO.SchDoc	
	Rev. 01	Page 11 of 30



	Title: AM0010 - B_PS_GT		
	A4	Number: B_PS_GT [No Variations]	Rev. 01
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 12 of 30
	Filename: B_PS_GT.SchDoc		



Title: AM0010 – CONFIG		
A4	Number: CONFIG [No Variations]	Rev. 01
Date: 20.10.2021	Copyright: Trenz Electronic GmbH	Page 13 of 30
Filename: CONFIG.SchDoc		

A

B

C

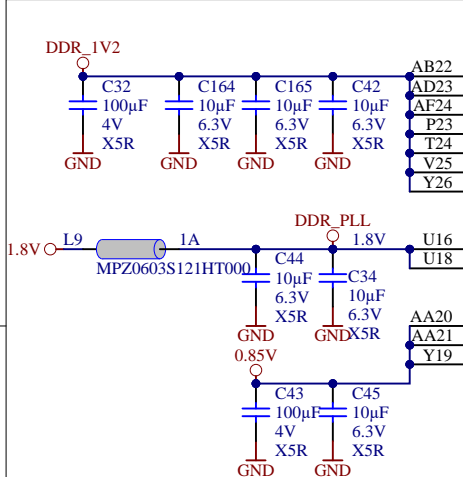
D

A

B

C

D



U11		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
VCC_PSDDR_PLL	PS_DDR_CS_N0_504	W27	DDR4-CS#
VCC_PSDDR_PLL	PS_DDR_CS_N1_504	V26	
VCC_PSDDR_PLL	PS_DDR_BA0_504	V23	DDR4-BA0
VCC_PSDDR_PLL	PS_DDR_BA1_504	W22	DDR4-BA1
VCC_PSDDR_PLL	PS_DDR_BG0_504	W24	DDR4-BG0
VCC_PSDDR_PLL	PS_DDR_BG1_504	V22	DDR4-BG1
VCC_PSDDR_PLL	PS_DDR_PARITY_504	V24	DDR4-PAR
VCC_PSDDR_PLL	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET#
VCC_PSDDR_PLL	PS_DDR_ACT_N_504	Y23	DDR4-ACT#
VCC_PSDDR_PLL	PS_DDR_ALERT_N_504	U25	DDR4-ALERT#
VCC_PSDDR_PLL	PS_DDR_ZQ_504	U24	
VCC_PSDDR_PLL	PS_DDR_ODT0_504	U28	DDR4-ODT0
VCC_PSDDR_PLL	PS_DDR_ODT1_504	U26	

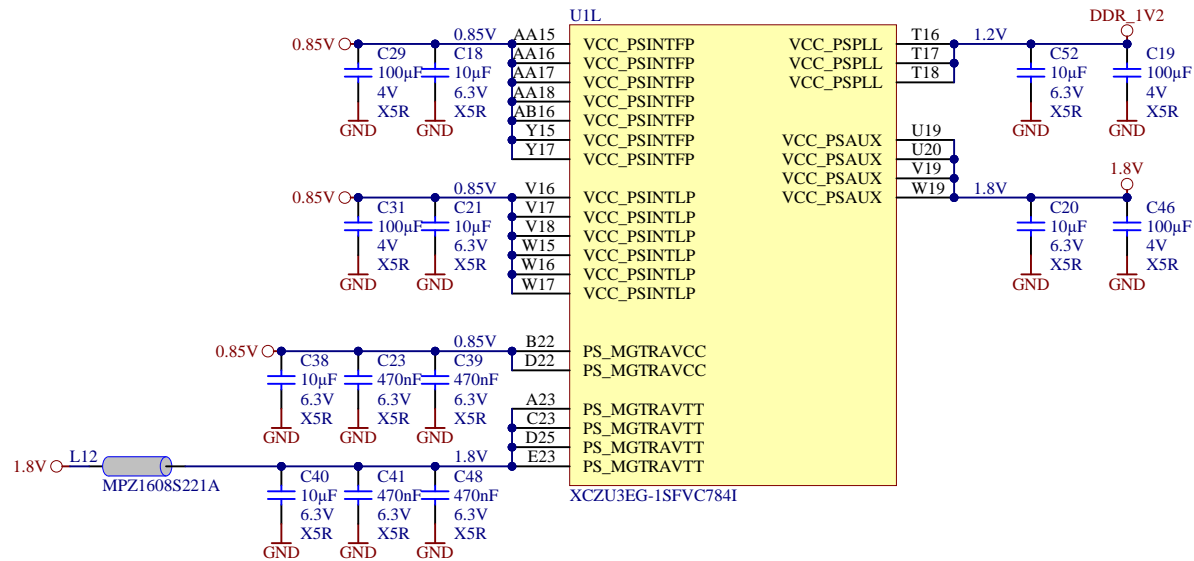
XCZU3EG-1SFVC784I


U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2_N	AG25	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7_P	J27	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7_N	J26	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
DDR4-DQS8_P	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
DDR4-DQS8_N	T27	PS_DDR_DQS_N8_504	

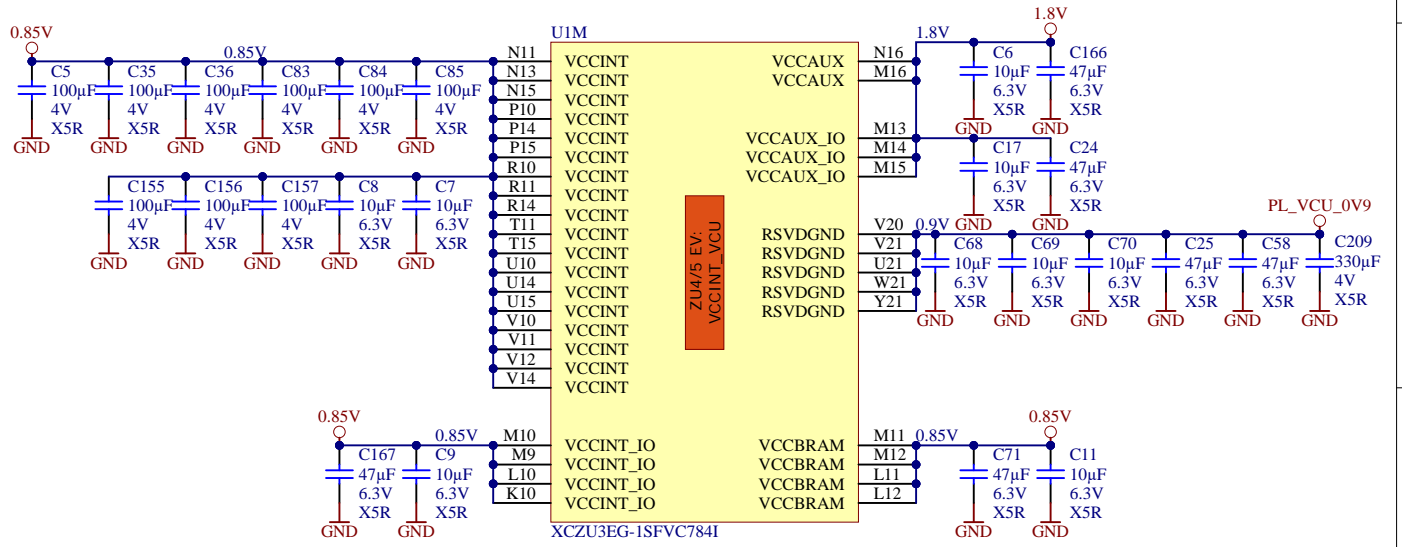
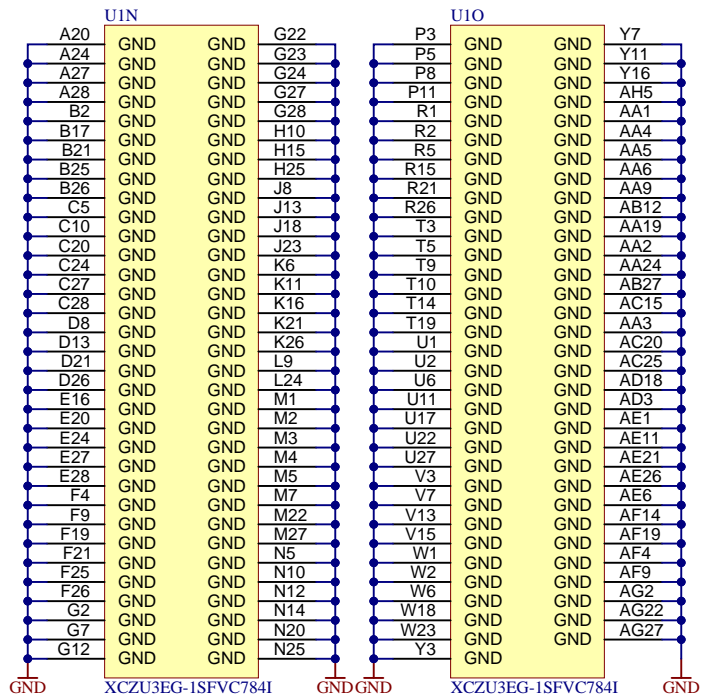
XCZU3EG-1SFVC784I




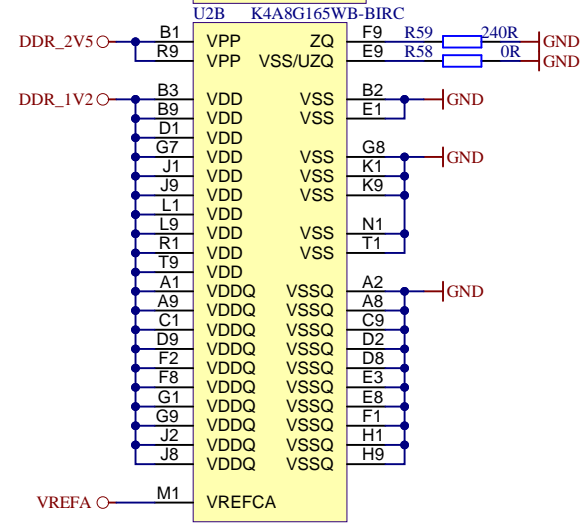
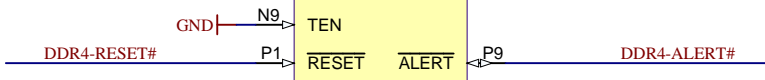
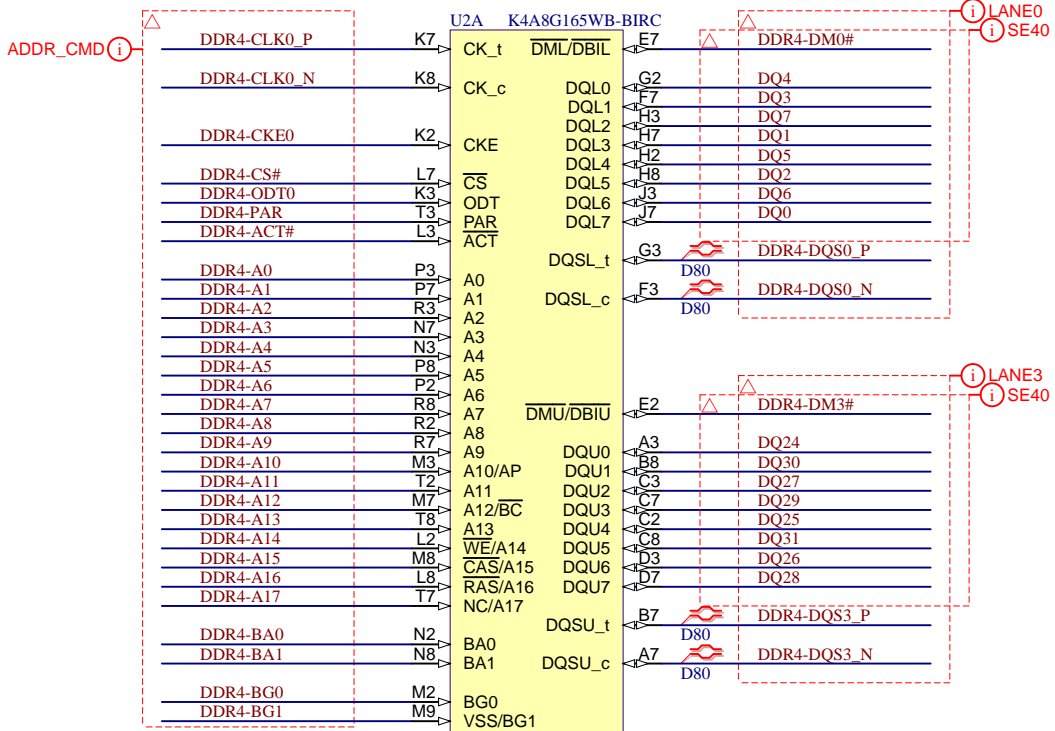
Title: AM0010 – PS_DDR		
A4	Number: PS_DDR [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 14 of 30
Filename: PS_DDR.SchDoc		



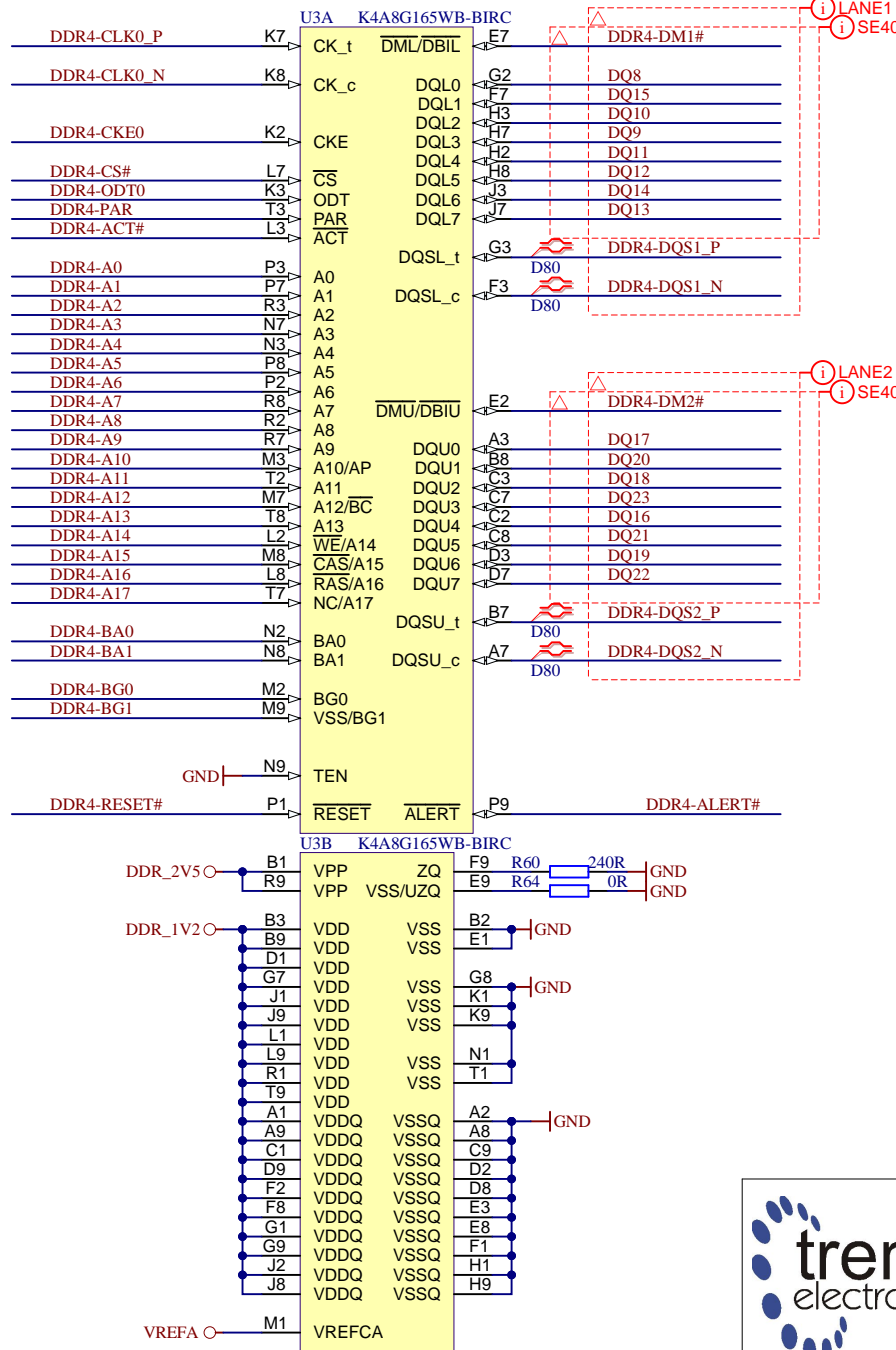

	Title: AM0010 – ZU_PS_POWER		
	A4	Number: ZU_PS_POWER [No Variations]	Rev. 01
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 15 of 30
	Filename: ZU_PS_POWER.SchDoc		



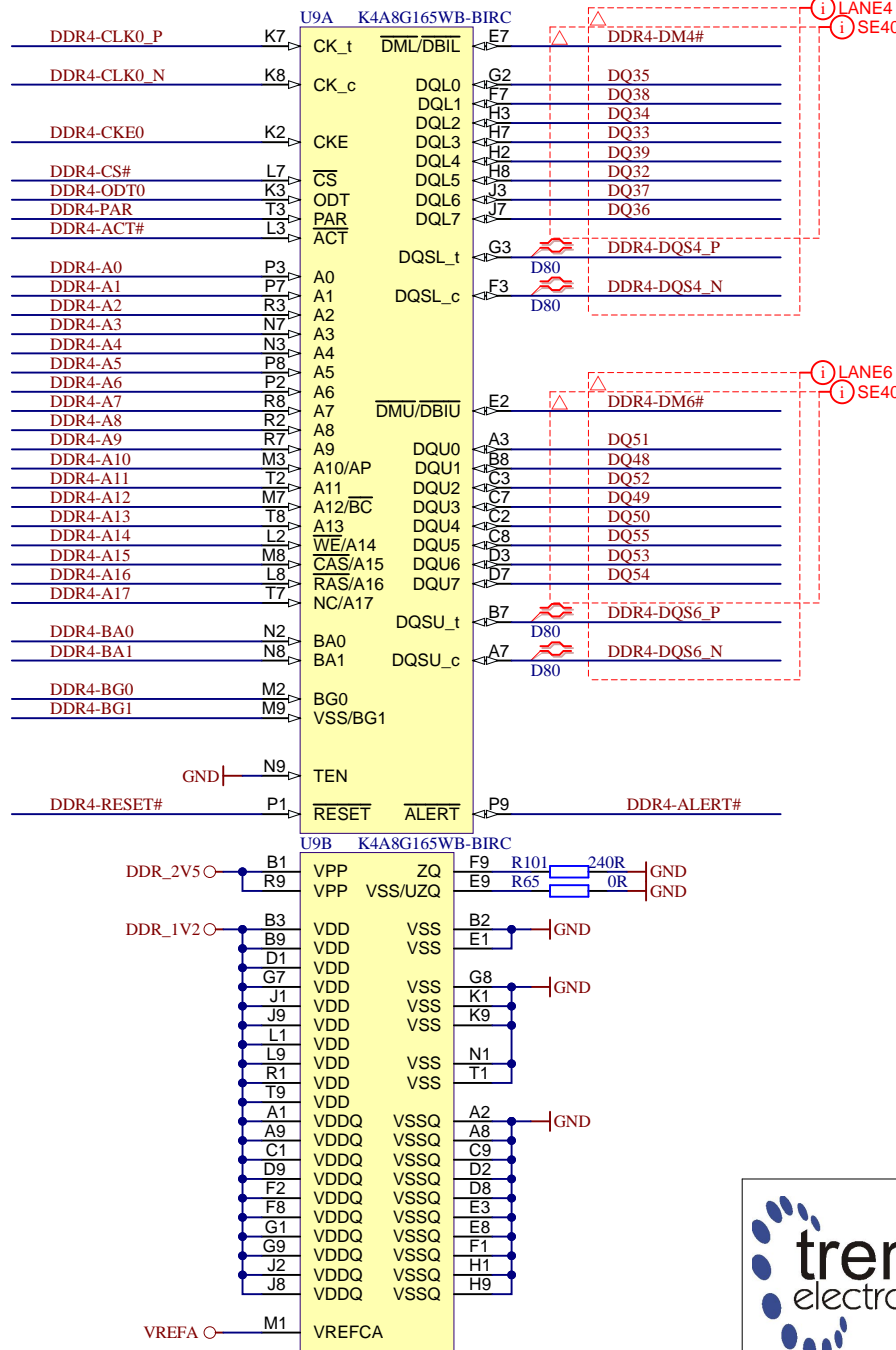
	Title: AM0010 – ZU_POWER	
	A4	Number: ZU_POWER [No Variations]
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH
	Filename: ZU_POWER.SchDoc	
	Rev. 01	Page 16 of 30




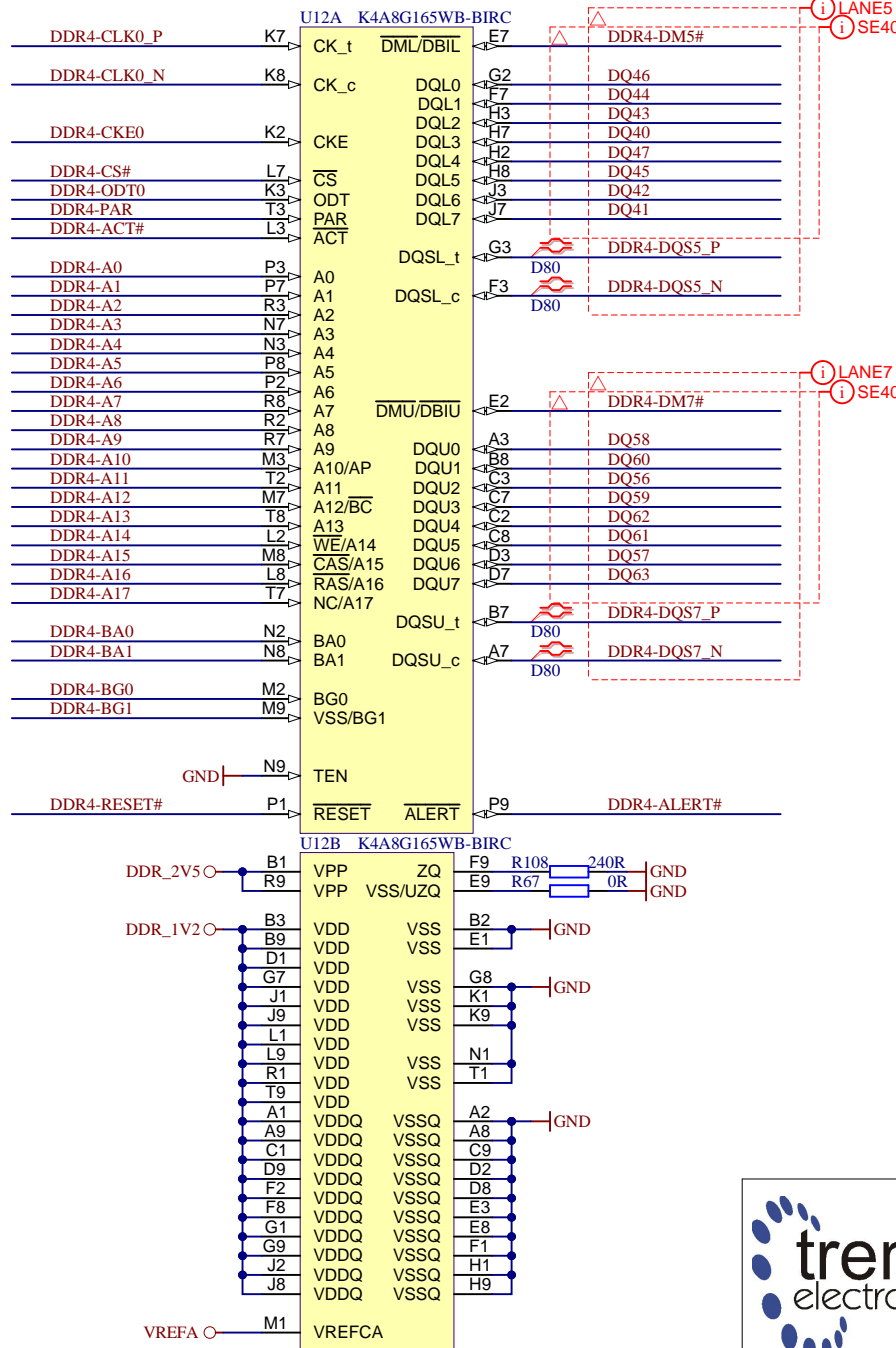

Title: AM0010 – DDR4-RAM		
A4	Number: DDR4-RAM [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 17 of 30
Filename: DDR4-RAM.SchDoc		

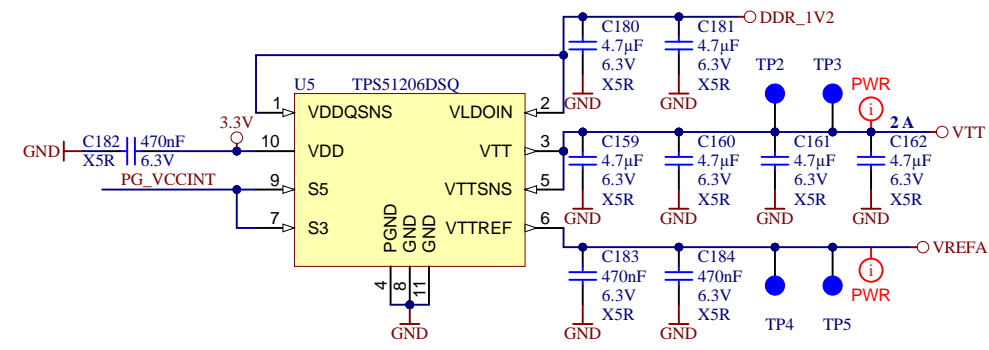
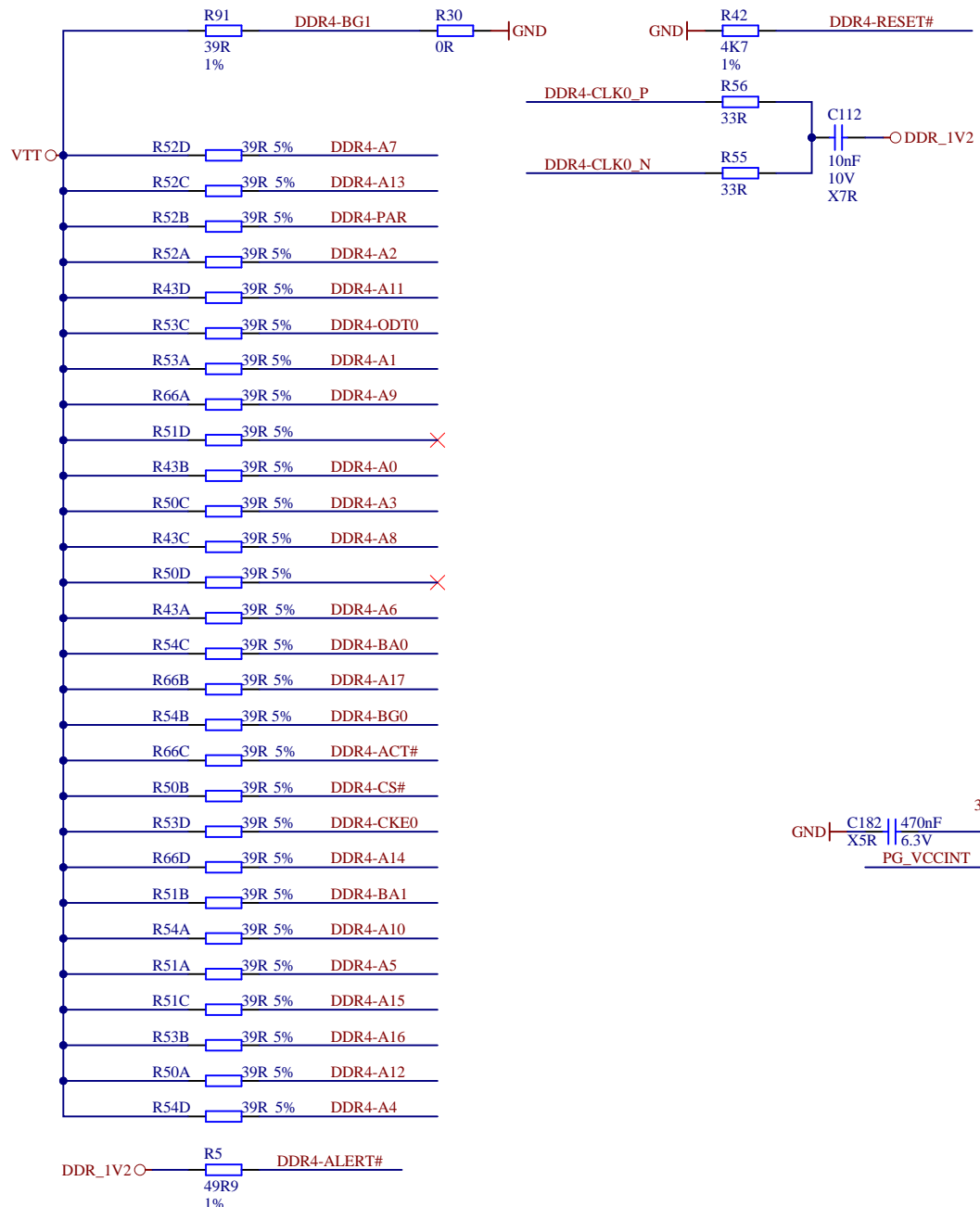
Title: AM0010 – DDR4-RAM_2		
A4	Number: DDR4-RAM_2 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 18 of 30
Filename: DDR4-RAM_2.SchDoc		



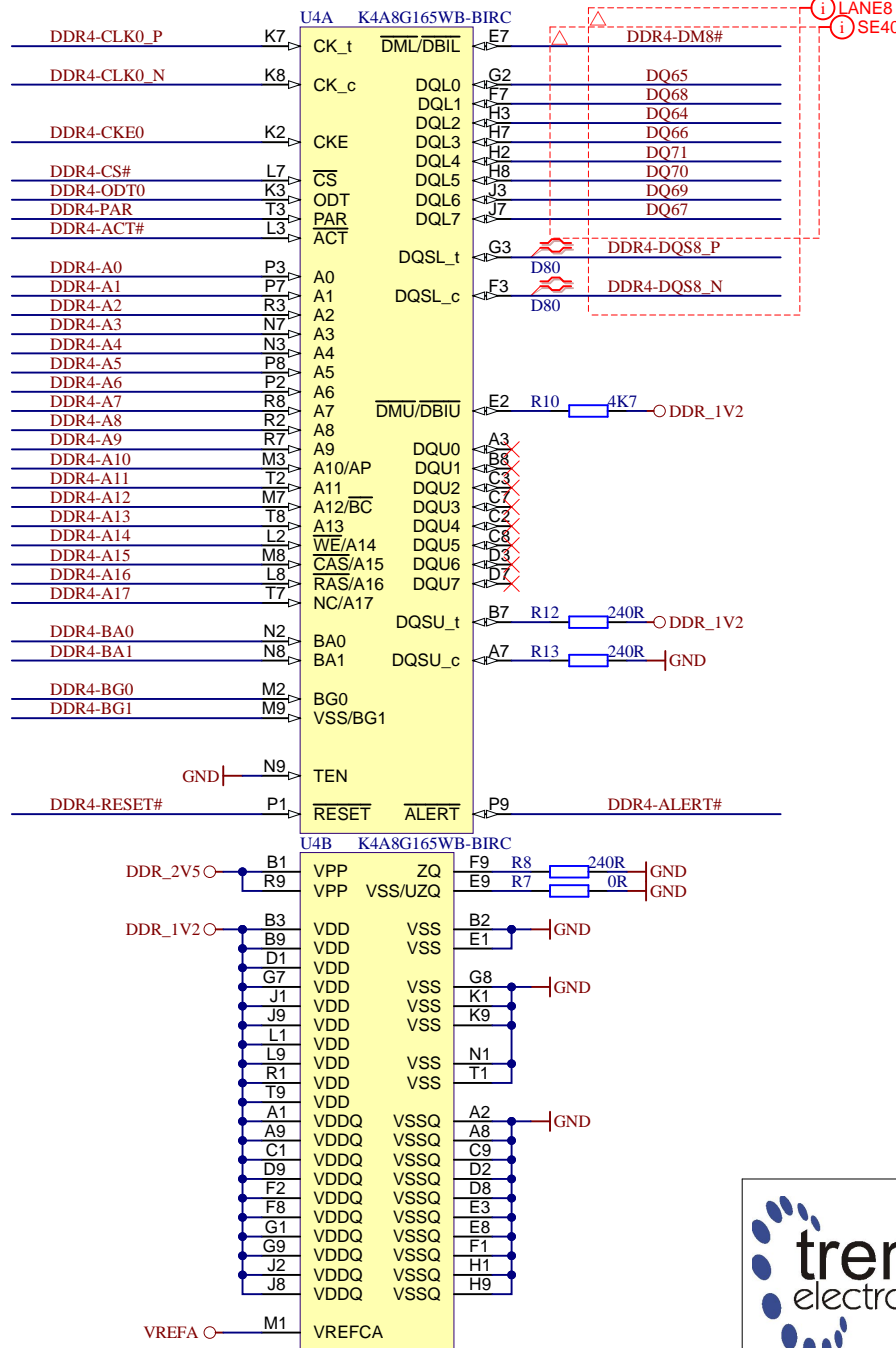

		Title: AM0010 – DDR4-RAM_3	
		A4	Number: DDR4-RAM_3 [No Variations]
Date: 04.10.2021		Copyright: Trenz Electronic GmbH	
Filename: DDR4-RAM_3.SchDoc		Page 19 of 30	

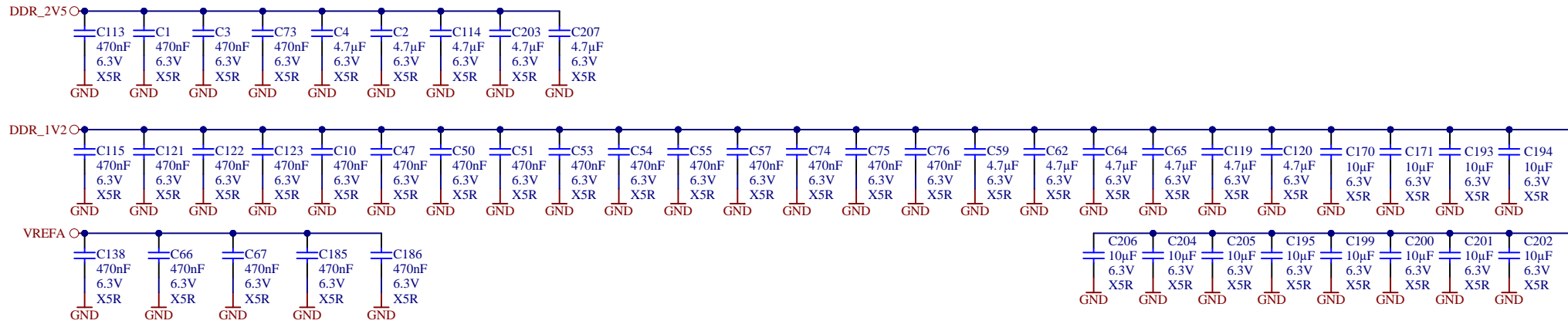
Title: AM0010 – DDR4-RAM_4		
A4	Number: DDR4-RAM_4 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 20 of 30
Filename: DDR4-RAM_4.SchDoc		




Title: AM0010 – DDR4-TERM		
A4	Number: DDR4-TERM [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 21 of 30
Filename: DDR4-TERM.SchDoc		

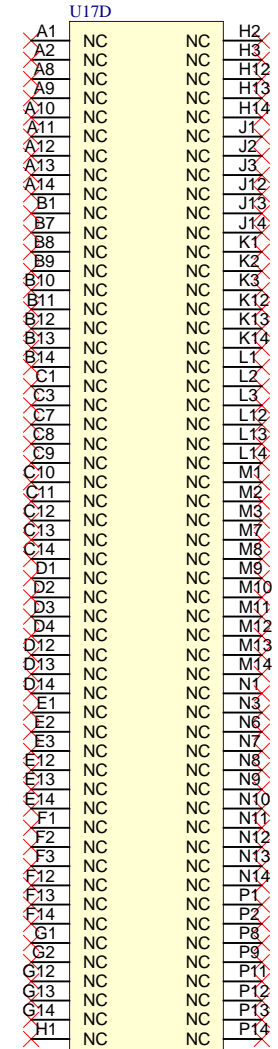
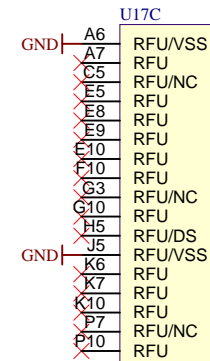
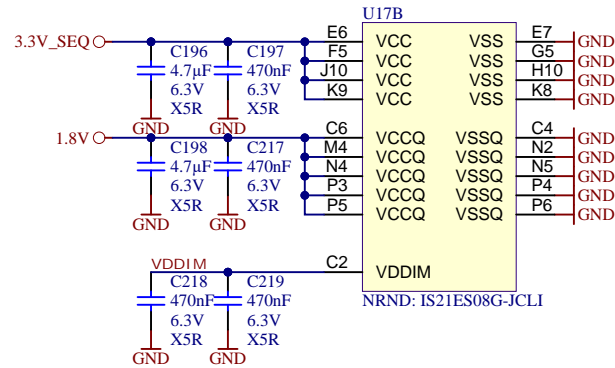
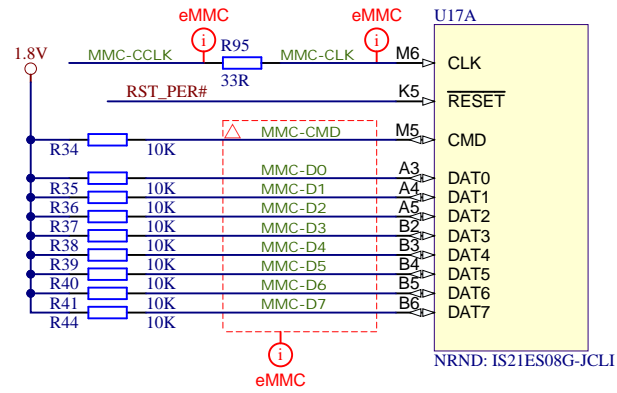



Title: AM0010 – DDR4-RAM_5		
A4	Number: DDR4-RAM_5 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 22 of 30
Filename: DDR4-RAM_5.SchDoc		

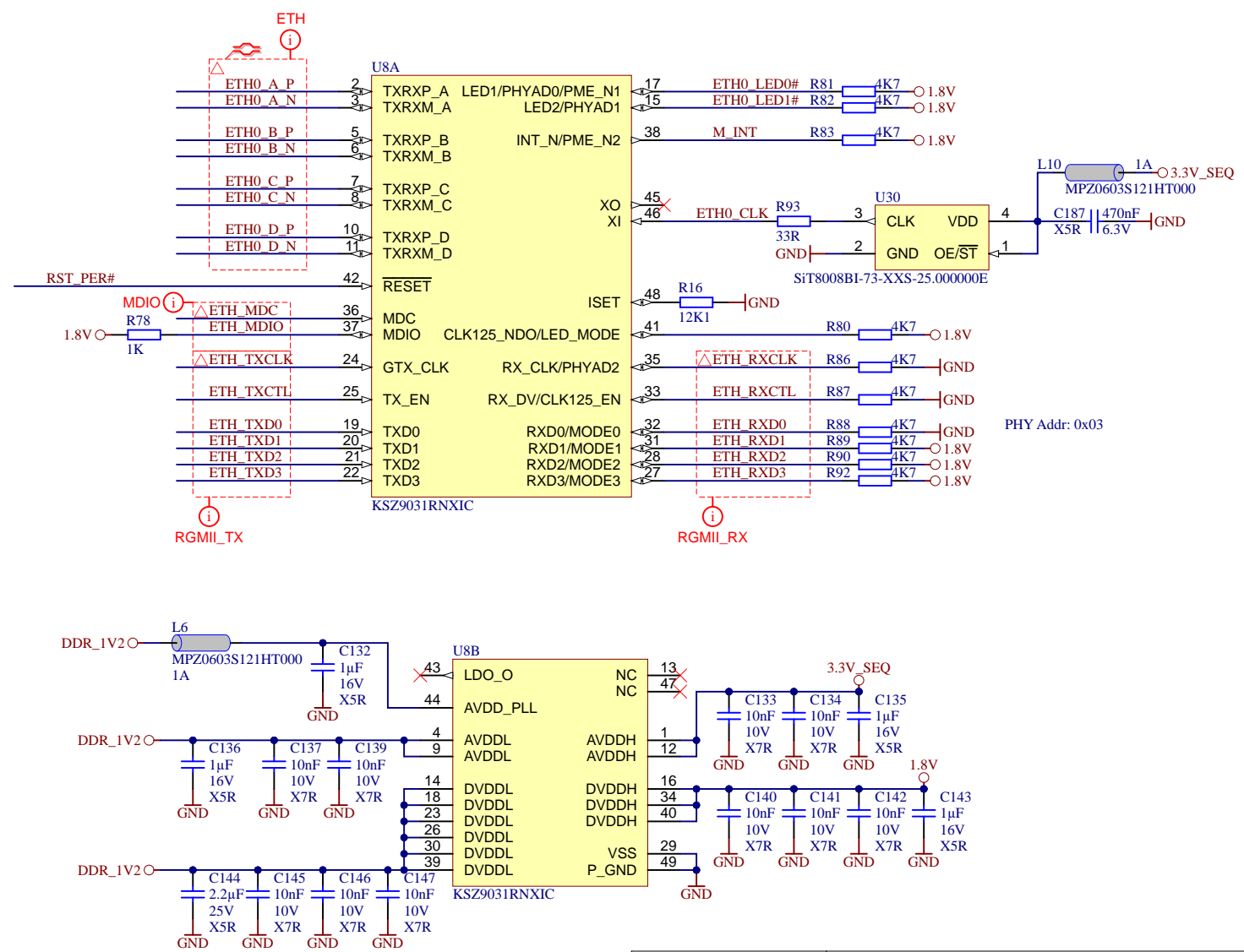



		Title: AM0010 – DDR4-CAPS	
		A4	Number: DDR4-CAPS [No Variations]
Date: 04.10.2021		Copyright: Trenz Electronic GmbH	
Date: 04.10.2021		Page 23 of 30	
Filename: DDR4-CAPS.SchDoc			

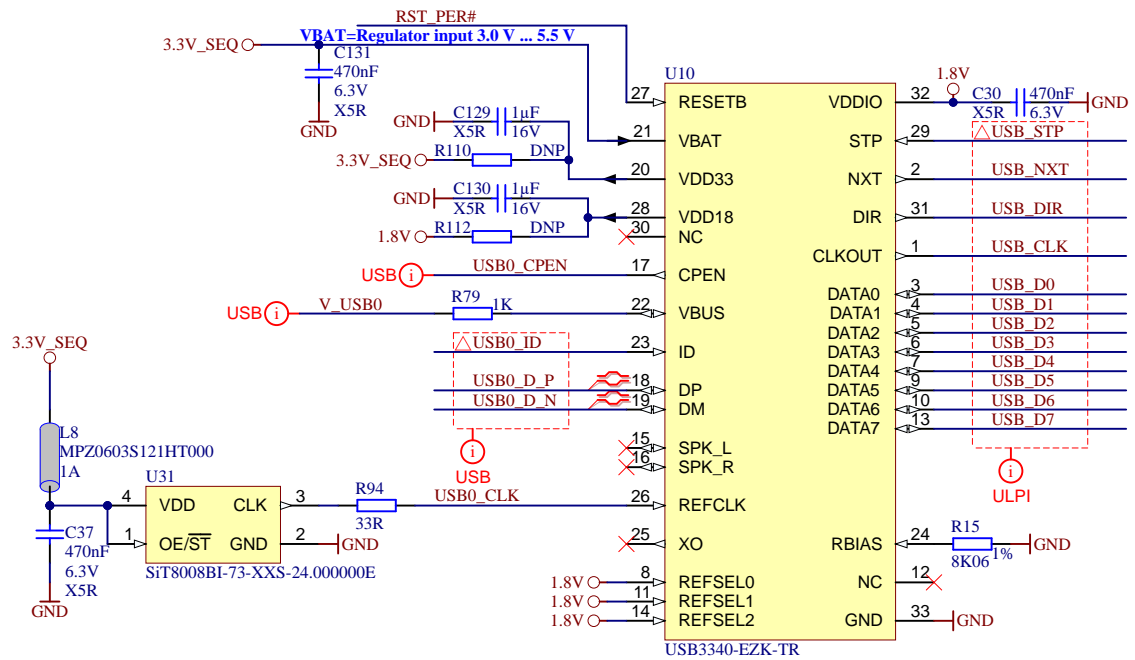
8GB eMMC



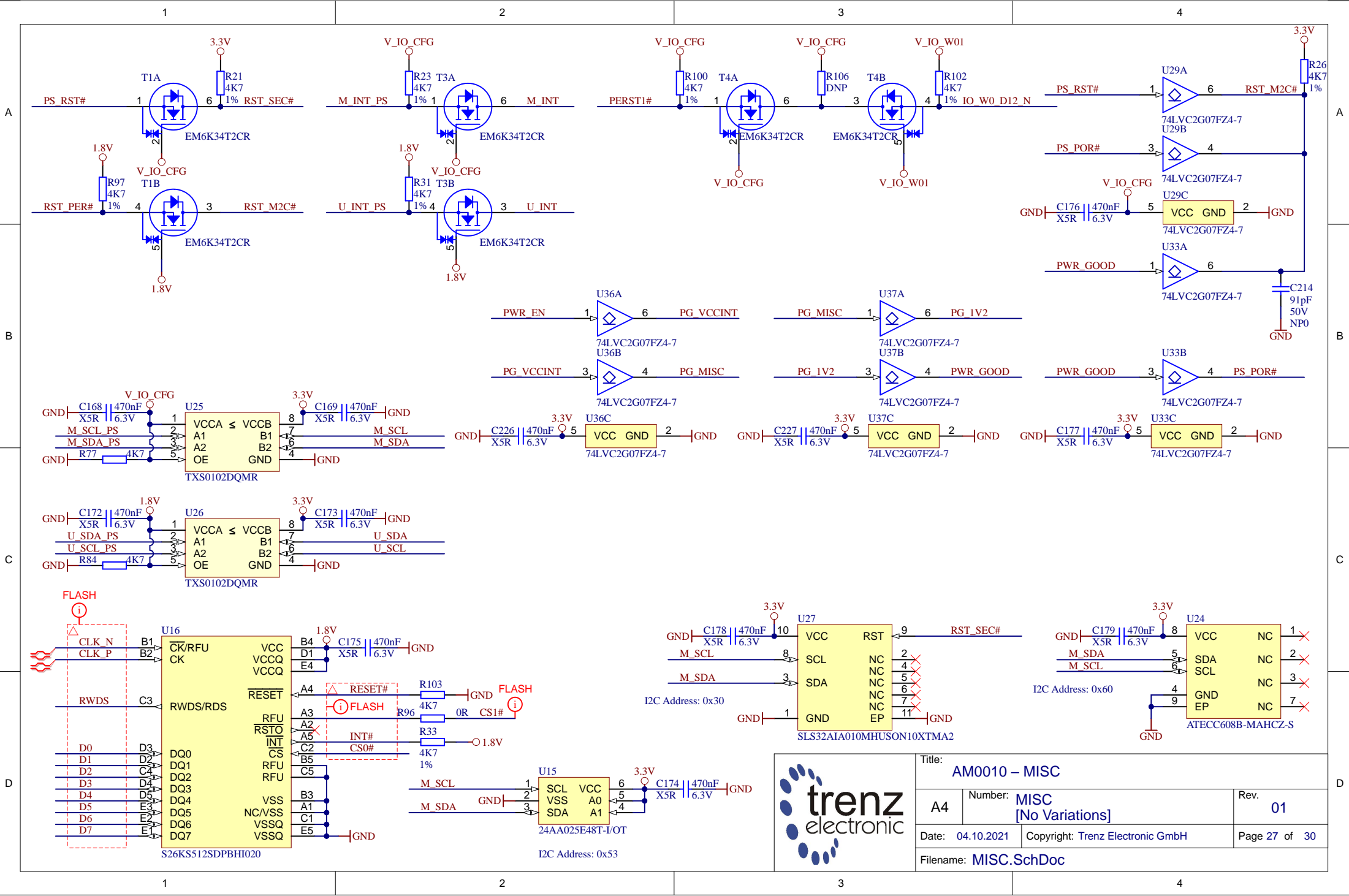
Title: AM0010 – eMMC		
A4	Number: eMMC [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 24 of 30
Filename: eMMC.SchDoc		



			Title: AM0010 – ETHPHY	
			A4	Number: ETHPHY [No Variations]
Date: 04.10.2021		Copyright: Trenz Electronic GmbH		Page 25 of 30
Filename: ETHPHY.SchDoc				

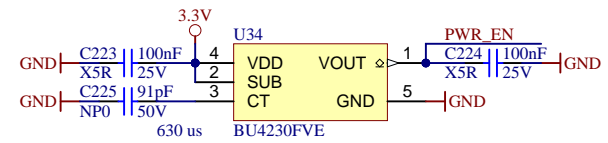
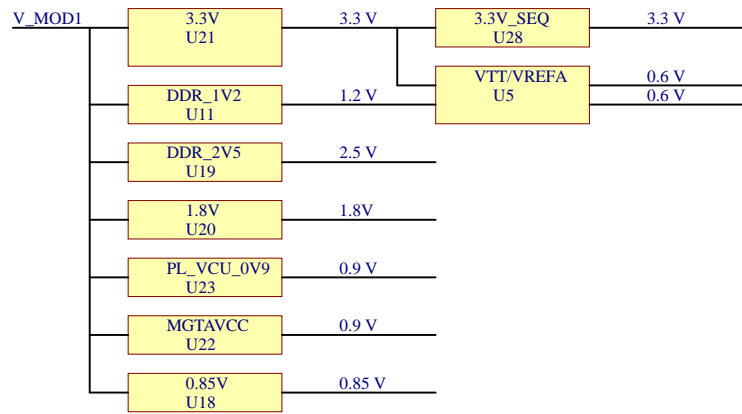


	Title: AM0010 – USBPHY	
	A4	Number: USBPHY [No Variations]
	Date: 04.10.2021	Copyright: Trenz Electronic GmbH
	Filename: USBPHY.SchDoc	
	Rev. 01	Page 26 of 30

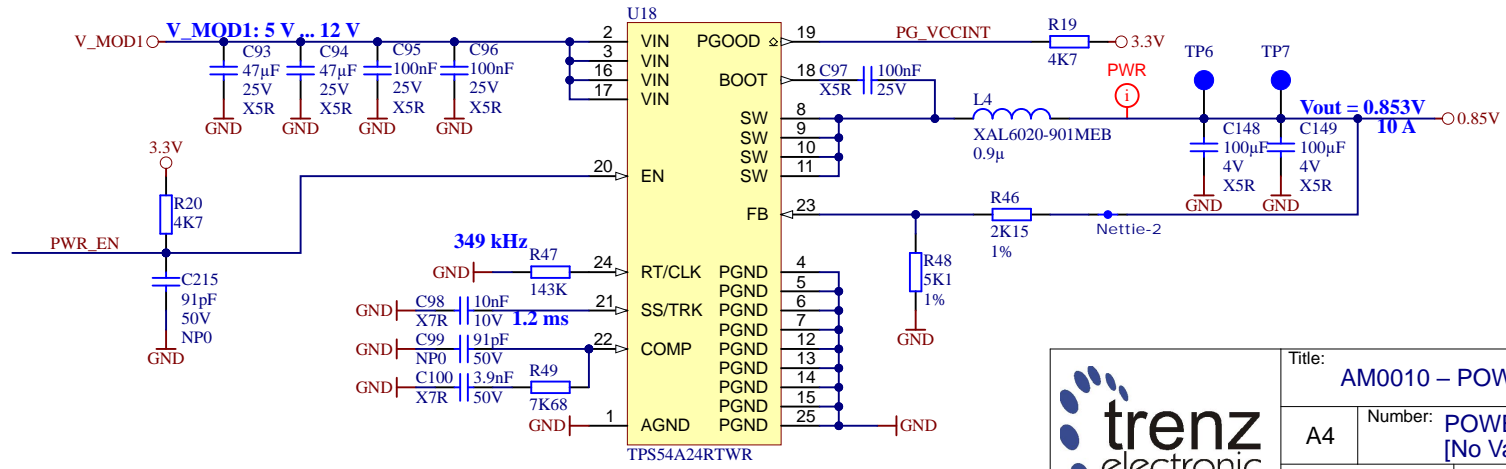
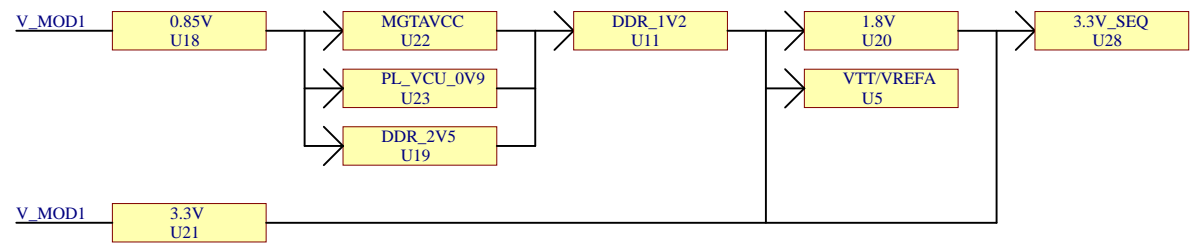


Title: AM0010 – MISC		
A4	Number: MISC [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 27 of 30
Filename: MISC.SchDoc		

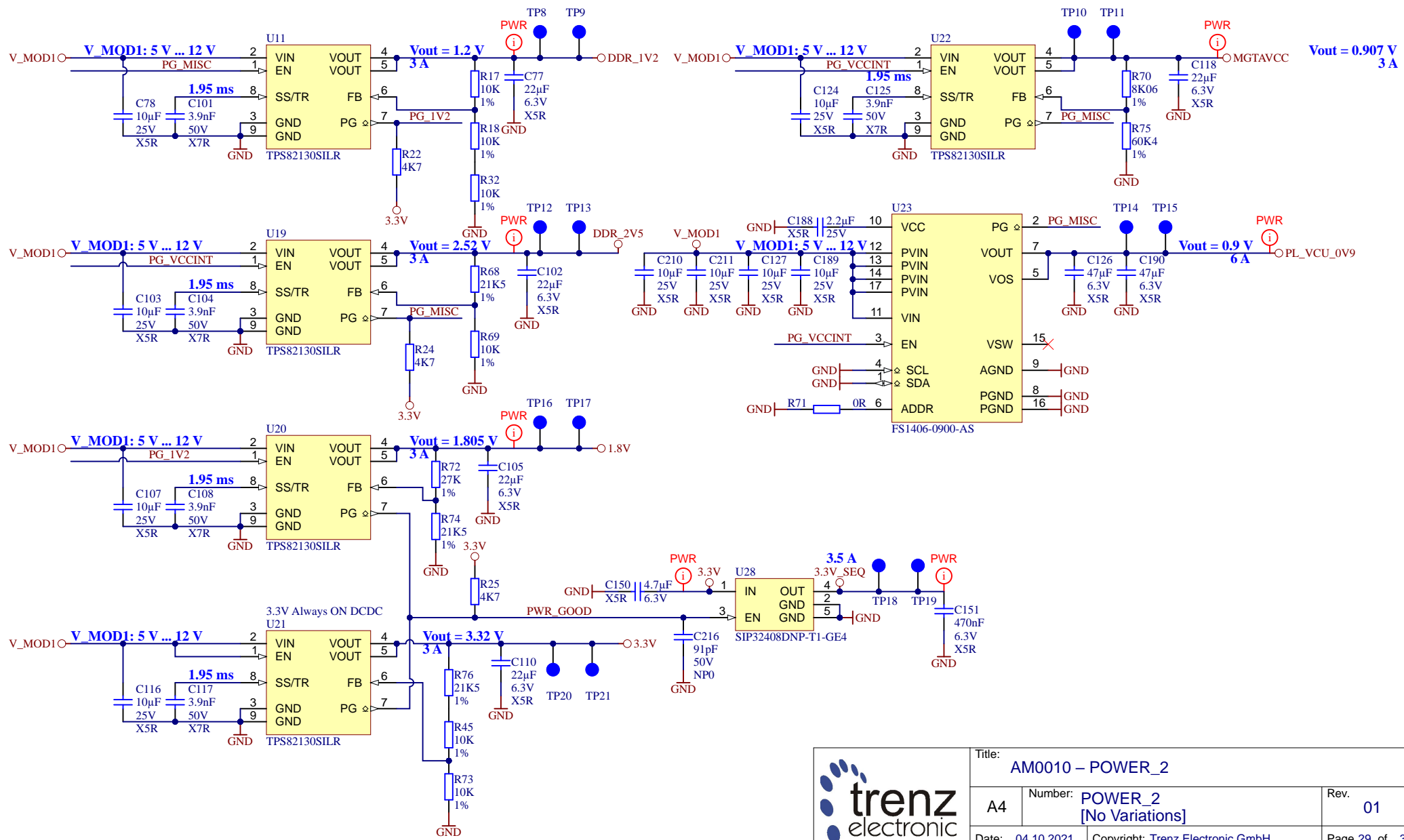
Power Supply Structure



Power Supply Sequencing



Title: AM0010 – POWER_1		
A4	Number: POWER_1 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 28 of 30
Filename: POWER_1.SchDoc		



Title: AM0010 – POWER_2		
A4	Number: POWER_2 [No Variations]	Rev. 01
Date: 04.10.2021	Copyright: Trenz Electronic GmbH	Page 29 of 30
Filename: POWER_2.SchDoc		

1

2

3

4

A

A

B

B


C

C

D

D

REV	Description	
-01	Initial revision	AL/ED

			Title: AM0010 – Revision_Changes					
			A4	Number: Revision_Changes [No Variations]		Rev. 01		
			Date: 04.10.2021		Copyright: Trenz Electronic GmbH		Page 30 of 30	
			Filename: Revision_Changes.SchDoc					

1

2

3

4